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Reg. No. : .....

Code No. : 30527 E Sub. Code : SSCA 4 A/ ASCA 41

... (CBCS) DEGREE EXAMINATION, APRIL 2022

Fourth Semester

Computer Applications

Skill Based Subject — MICROPROCESSOR

(For those who joined in July 2017 onwards)

...me : Three hours Maximum : 75 marks

PART A — (10 × 1 = 10 marks)

Answer ALL questions.

Choose the correct answer :

Which of these is the architecture of microprocessor?

(a) CISC (b) RISC

(c) Both (a) and (b) (d) None of these

2. RISC stands for

(a) Reduced Instruction Set Computer

(b) Reduced Integrated Set Computer

(c) Resource Instruction Set Computer

(d) Resource Instruction System Computer

3. ALE demultiplexes the ———— and ————

(a) Data bus, low order address bus

(b) Data bus, high order address bus

(c) Data bus, address but

(d) All of the above

4. 8085 microprocessor zero flag is set if ———— results zero.

(a) I/O operation (b) Memory operation

(c) Mux operation (d) ALU operation

5. The ———— ensures that only one IC is active at a time to avoid a bus conflict caused by two ICs writing different data to the same bus.

(a) Control bus

(b) Control instructions

(c) Address decoder

(d) CPU

The technique of assigning a memory address to each I/O device in the computer system is called

a) memory – mapped I/O

b) ported I/O

c) dedicated I/O

d) wired I/O

A computer program that converts an entire program into machine language at one time is called a/an

(a) Interpreter (b) Simulator

(c) Compiler (d) Commander

The advantage of RISC processor over CISC processor is that

(a) The hardware architecture is simpler

(b) An instruction can be executed in one cycle

(c) Less number of registers accommodate in chip

(d) Parallel execution capabilities

What is the output of the following code PUSH AL?

(a) Decrement SP by 2 and push a word to stack

(b) Increment SP by 2 and push a word to stack

(c) Decrement SP by 2 and push an AL to stack

(d) Illegal

10. What is the function of watchdog timer?

(a) The watchdog timer is an external timer that resets the system if the software fails to operate properly

(b) The watchdog timer is an internal timer that sets the system if the software fails to operate properly

(c) The watchdog timer is an internal timer that resets the system if the software fails to operate properly

(d) None of them

PART B — (5 × 5 = 25 marks)

Answer ALL questions, choosing either (a) or (b).

Each answer should not exceed 250 words.

11. (a) Explain the functions of flags in 8085 microprocessor.

Or

(b) Write a brief note on Z-80 microprocessor.

12. (a) Explain the term : Instruction cycle.

Or

(b) Explain the timing diagram for opcode fetch.

13. (a) Explain what is vectored interrupt.

Or

(b) Discuss the function of DMA data controller 8257.

14. (a) Explain how an A/D converter can be realized employing a D/A converter.

Or

(b) Write a note on display interface.

15. (a) What are co-processors? Explain with example.

Or

(b) Explain the importance of multi bus.

PART C — (5 × 8 = 40 marks)

Answer ALL questions, choosing either (a) or (b).

Each answer should not exceed 600 words.

16. (a) Draw the architecture of 8085 microprocessor and explain the functions of each block.

Or

(b) Explain in detail the various addressing modes in 8085 microprocessor.

17. (a) With suitable diagrams, explain the timing diagram for memory read and write cycle.

Or

(b) Write a assembly language program to add two 8-bit numbers, the sum may be of 16 bits.

18. (a) Explain the different operating modes of 8255A PPI.

Or

(b) Describe the programmable interrupt controller 8259.

19. (a) Explain the interfacing of A/D converter to 8085 microprocessor.

Or

(b) Explain the interfacing techniques of stepper motor with 8085 microprocessor.

20. (a) Give detail account on bus interface controller.

Or

(b) Explain the following :

(i) RS232 bus standard and

(ii) GPIO.

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